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An FPGA application of home security code using verilog

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ABSTRACT

Traditional entrance keys performed a number of drawbacks, including the ease with which they can be stolen, duplicated, or misplaced, allowing unauthorized people to gain access to cash, valuables, and other important documents. As known, most digital electronic entrance locks use application specific integrated circuits (ASICs) as based, which have the disadvantage of being unable to be reconfigured, as opposed to field programmable gate arrays (FPGA). This project proposed a home security code lock using verilog hardware descriptive language (HDL) with two unlocking modes, using a button or a keypad which can be changed using a switch. The 7-segment on the Altera DE2-115 trainer board is used to display the passcode press by the keypad. The result of simulation on the keypad using finite state machine (FSM) technique was fulfill the theoretical concept in which it will go to the next state each time the correct input or passcode was entered. When the wrong input or passcode was entered, it will be entered to reset mode. As the conclusion, a fully comply output according to the theoretical FSM concept is fully achieved in this project.

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1. INTRODUCTION

The security system in the past was mechanical, consisting of a plain wall or a wall with a watchdog [1]. In our day-to-day lives, security is a major concern, and access control systems were an important link in the security chain [2]. People access their households and workplaces frequently every day and there are many problems associated with security and accessibility [3]. Even though urbanization and the frequency of criminal activities had increased in recent decades, the old-fashioned key-and-lock method is still commonly utilized in today's guard system, posing security and efficiency issues [4], [5]. The effectiveness of the old-fashioned key and lock method may be jeopardized because the keys are vulnerable to being misplaced or duplicated [6]. Nowadays, with the urbanization and miscellaneous criminal types, the efficiency of the key-and-lock has been challenged [7]. The digital lock system plays a vital role in providing security and reducing personnel in the home and building automation situation [8]. It is necessary to reprogram by an electronic door lock rather than replace the whole physical key lock in which obviously is cost saving [9]-[11] and reduce time [12], [13].

Microcontrollers and microprocessors were used in the new generation security system, which provide 100 percent theft and burglary resistance [2]. Several development platforms have been designed to meet the hardware and software needs of such applications, especially since they require large-scale data processing. For that purpose, reconfigurable architectures such as FPGAs is increasingly used due to their

high flexibility [14]. Field programmable gate arrays (FPGA) is another alternative for embedded systems in which trial and error is possible, does not have a fixed instruction set and process instruction in parallel processing. The biggest advantage of using the FPGA device as a new component in the industrial environment is that the different hardware features of FPGA (flexible and reusable integrated circuit, computing parallel tasks, cost efficiency and multiple input/output capability) that can be designed by a developer for different application platforms after production [15]. FPGA can provide a wide opportunity for modern applications. On the contrary, application specific integrated circuits (ASIC) is unable to be reprogrammed, limited capabilities and much rely on the sequential process. This is because it is designed for one sole purpose and they function the same their whole operating life [16]. An Arduino UNO using ATMEGA328P chip as microcontroller, the input and output of the electronic digital lock system using 4x4 matrix keypad, LCD 16x2 and a buzzer connected with the Arduino UNO [1]. Another aspect point to ponder is FPGA was found to be more efficient in terms of execution time and less space than the other platforms mentioned above [17]. FPGA-based systems are more suitable to control technique which requiring parallel performing [18], [19]. Currently, FPGA have received huge attention of researchers due to their relatively high performance, low power consumption, reconfigurability and fast development round [20]. The keyless lock system was a security feature that only allowed the house owner to unlock the door by sliding the secret code on the Altera DE2-115 trainer board's slide switches [6]. It's not very user-friendly to use a switch as a passcode input. Home security code lock system presented by Saleh [21], was almost identical to the FPGA application on a smart home security system in which using FPGA for the system with add-on Arduino UNO for the temperature sensor LM35 and servo motor as the entrance access [22].

Finite state machine (FSM) is a sequential circuit that controls number of inputs by following a pre-defined number of states, each of which is a stable entity that can occupy several states [1]. the research in [23]-[25], utilized the FSM approach, which uses a Xilinx board and ModelSim to allow the lock to only open when the desired passcode was entered or the specified sequence is detected by the system using a keypad [23]-[25].

In this project, an Altera DE2-115 trainer board will be used as the brain of the home security code lock system. The objectives of this project are to design digital hardware circuit of home security code lock using verilog hardware descriptive language (HDL). Then, the process of verifying the functionality on the digital hardware circuit of home security code lock was being done using ModelSim. Later, the performance is verified by downloading the design onto the Altera DE2-115 trainer board. In this project, a button and a keypad will interact as the way to unlock the entrance which user can changing this unlocking method using a single switch.

2. RESEARCH METHOD

Figure 1 shows the design flow of methodology for this home security code lock using verilog HDL. During design, verification and simulation process, the first step was designing the digital circuits of home security code lock system using verilog HDL. Next step, verify the design whether it was following the desired output or not via ModelSim. Then, using Quartus II Pin planner to assign device I/O pins [26]. After that, upload into the board and project testing to check whether the result was as expected or not.

The flowchart method for home security code lock system is shown in Figure 2. The system includes two unlocking methods to open the home entrance, as previously mentioned. If the user does not turn on the switch, only the push button will work, which means the keypad will not work even if the keypad was pressed. If switch was off, the green LED will only light up when the pushbutton was pressed. Meanwhile if the switch was on, 7-segment will display “L” and Red LED will light up toindicate the door still is still lock. Only when the correct passcodewhich were “2, 6 and C”, then only the 7-segment will display “U” and Green LED will light up to indicate the door is unlocked.

A 4x4 matrix membrane keypad is used in this work as shown in Figure 3. Figure 4 illustrates the circuit schematic connection rows and columns of the keypad. As for the function operation of the keypad, the button will detect when both of a row and column detected at falling edge. Table 1 provides the values for the rows and columns for the button that was detected as being pressed. For example, button number 4 when C1 of the column is zero and R2 of the row is zero.

Figure 5 illustrates the top module design of home security code lock implemented in the DE2-115 using verilog HDL. Inside of the top module, there were 3 sub-modules, decoder, FSM and display controller. The role of sub-module decoder was to decode the input from the keypad. Next sub-module was FSM which only effect when keypad was using to unlock the home entrance. Last sub-module was display controller that display the 7-segment to indicate user the digit that were entering, which also only effect when using keypad to unlock the home entrance.

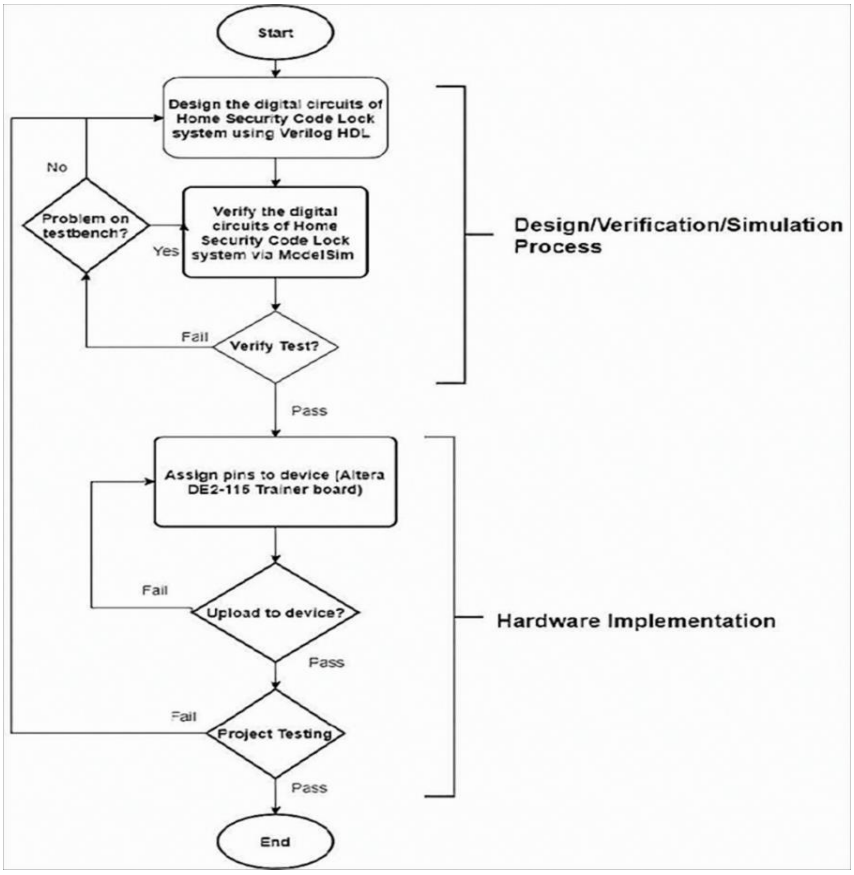


Figure 1. Design flow of methodology

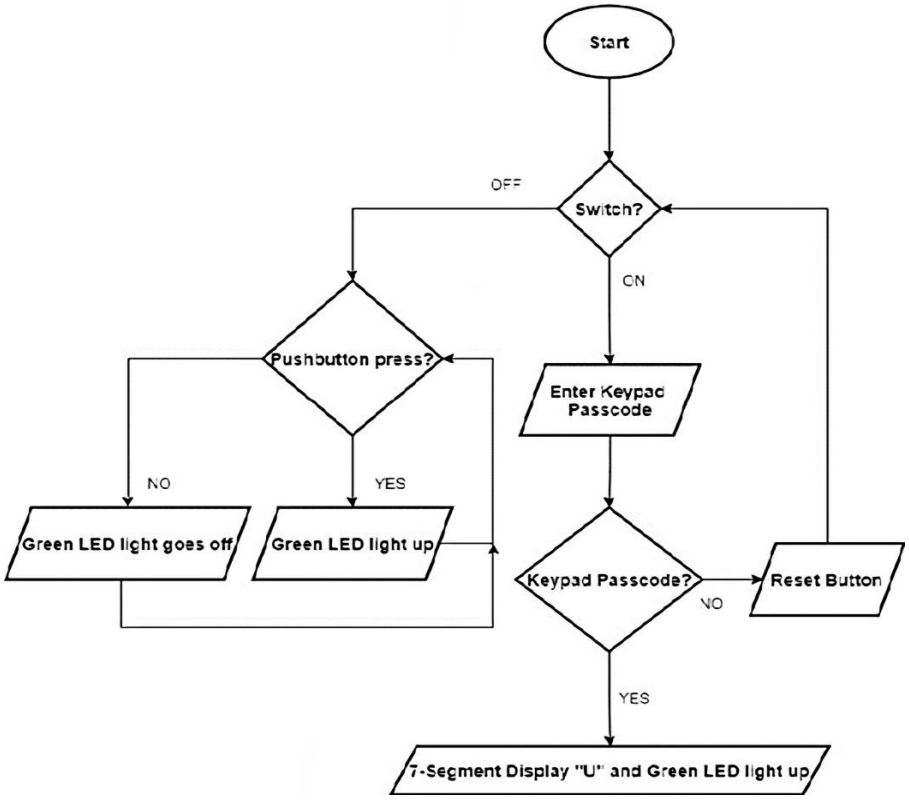


Figure 2. Flowchart process of home security code lock

Figure 3. 4x4 Matrix membrane keypad

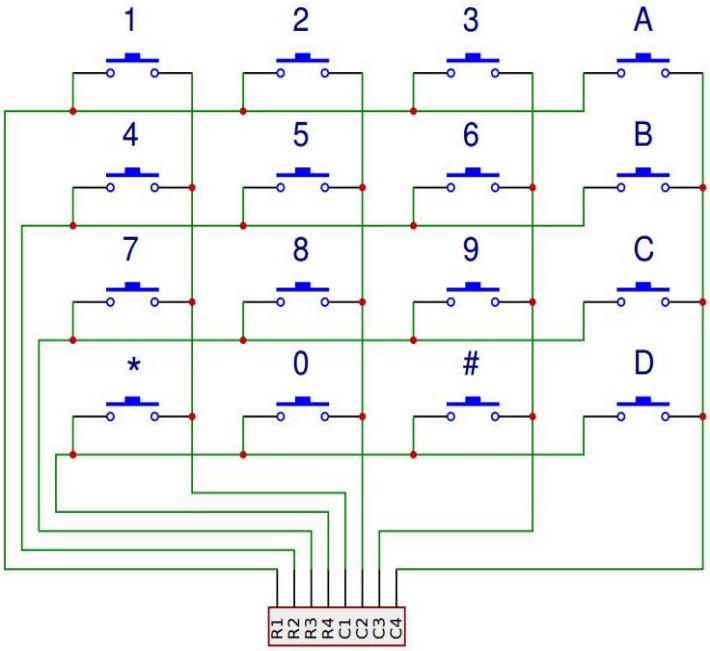


Figure 4. Schematic layout of 4x4 keypad

Table 1. Columns and rows

Column (C1, C2, C3, C4)	Row (R1, R2, R3, R4)	Button
0111	0111	1
0111	1011	4
0111	1101	7
0111	1110	*
1011	0111	2
1011	1011	5
1011	1101	8
1011	1110	0
1101	0111	3
1101	1011	6
1101	1101	9
1101	1110	#
1110	0111	A
1110	1011	B
1110	1101	C
1110	1110	D

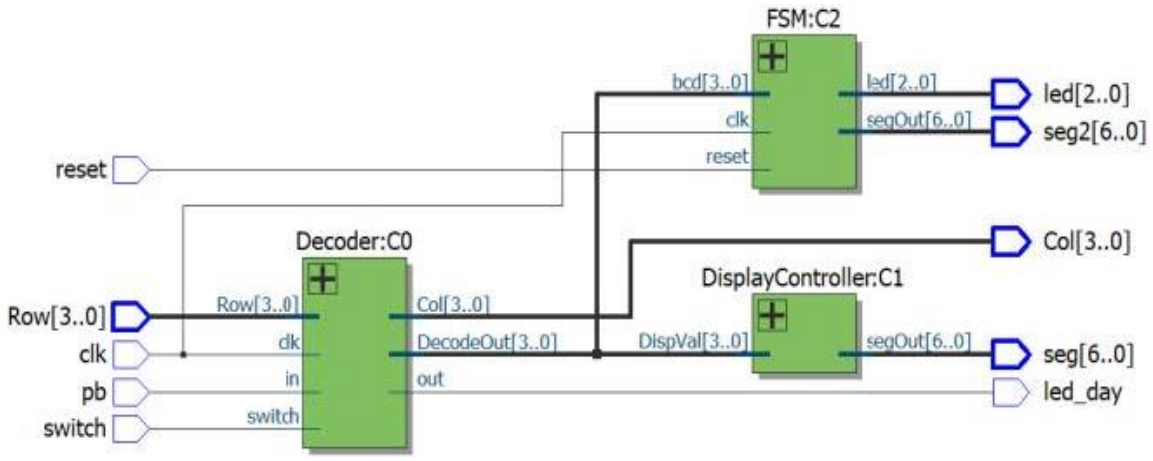


Figure 5. Top module of home security code lock

3. RESULTS AND DISCUSSION

3.1. Finite state machine

Figure 6 shows the state diagram for home security code lock using verilog HDL. It had 4 states which were IDLE, S1, S2 and S3. IDLE state represents when home entrance was lock while S3 when home entrance was unlocking. Transition from IDLE to S1 was 2, from S1 to S2 was 6 and from S2 to S3 was C. To return default state was by using the reset button.

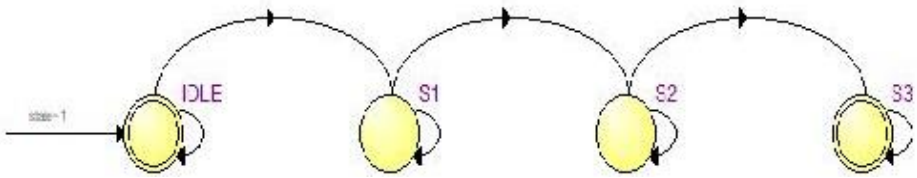
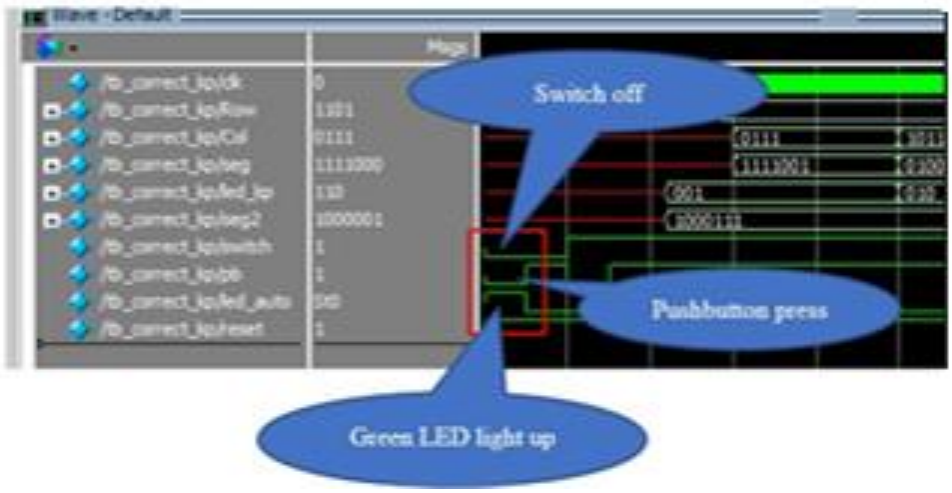


Figure 6. State diagram for home security code lock

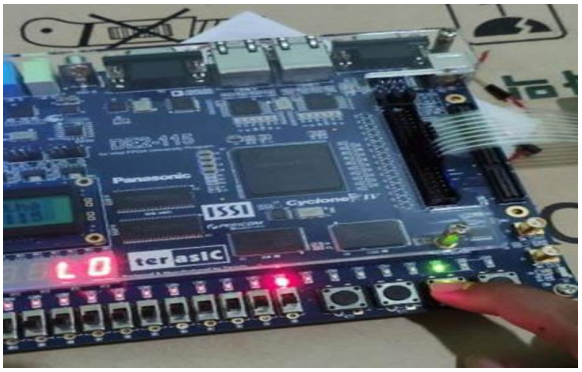
3.2. ModelSim simulation and DE2-115 verification

3.2.1. Switch off and pushbutton pressed

According to Figure 1, the project testing is as shown in Figure 7. Figure 7(a) in which show the timing diagram and the output from DE2-115. Figure 7(b) represents when the switch was off and button was press in which caused the Green LED to light up. Button in DE2-115 was active low which means the button should be in falling edge.



(a)

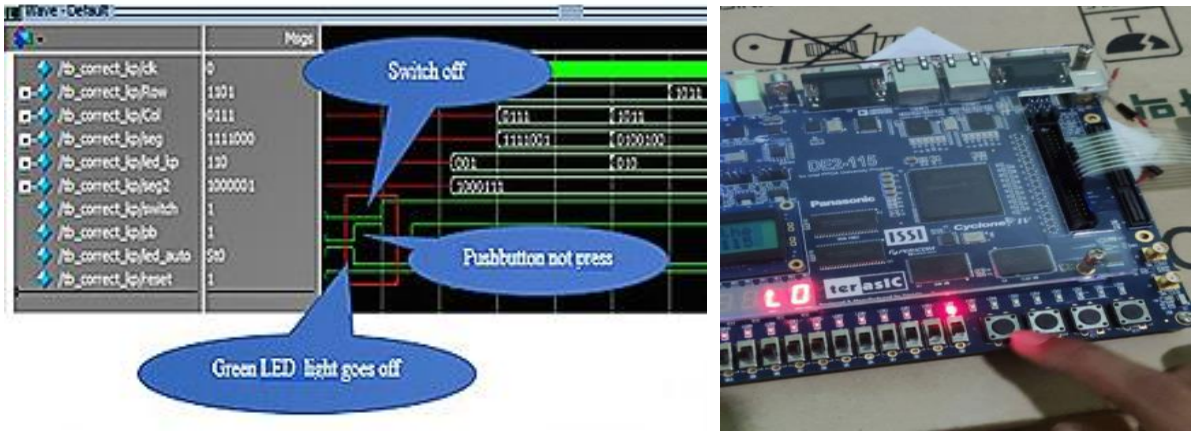


(b)

Figure 7. Simulation and verification when switch off and pushbutton was pressed with (a) ModelSim simulation and (b) Altera DE2-115 verification

3.2.2. Switch off and pushbutton unpressed

According to Figure 1, the project testing is as shown in Figure 8. Figure 8(a) in which show the timing diagram and the output from DE2-115. Figure 8(b) represents when the switch was off and button was not pressed in which caused the Red LED to light up. Button in DE2-115 was in rising edge means the button was not pressed and Green LED off.

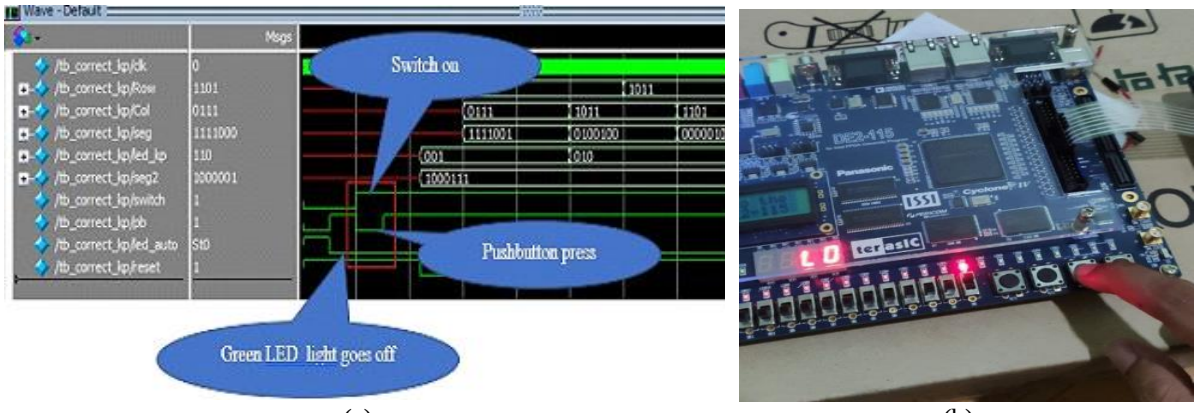


(a) (b)

Figure 8. Simulation and verification when switch off and pushbutton was unpressed with (a) ModelSim simulation and (b) Altera DE2-115 verification

3.2.3. Switch on and pushbutton pressed

According to Figure 1, the project testing is as shown in Figure 9. Figure 9(a) in which show the timing diagram and the output from DE2-115. Figure 9(b) demonstrates that when the switch was turned on, the button did not work even when pressed, and the Green LED light off since the final state of the Green LED had gone off before the switch was turned on. Then, using a keypad as an input, unlock the home entrance with a code lock.



(a) (b)

Figure 9. Simulation and verification when switch off and pushbutton was pressed with (a) ModelSim simulation and (b) Altera DE2-115 verification

3.2.4. Switch on and keypad correctly pressed

Figure 10 shows the output for the ModelSim simulation when the sequence of the keypad had been correctly pressed using the sequence of "2", "6" and "c". The initial state is entered using reset button. Figure 11 reflects the outcome of "L2" meaning that "Locked 2" on the Altera DE2-115 trainer board verification when keypad of "2" was correctly pressed. Figure 12 demonstrates the outcome of "L6" meaning that

"Locked 6" on the Altera DE2-115 trainer board when keypad of "6" was pressed. Finally, Figure 13 shows the outcome of "UC" stands for "Unlocked C" on the Altera DE2-115 trainer board when keypad of "C" was pressed. The "U" will notify that all the previously entered combination was correct and the system will be in "unlocked" or reset state. Table 2 and Table 3 are the summary on the results that had been obtained from Figure 7 until Figure 12.

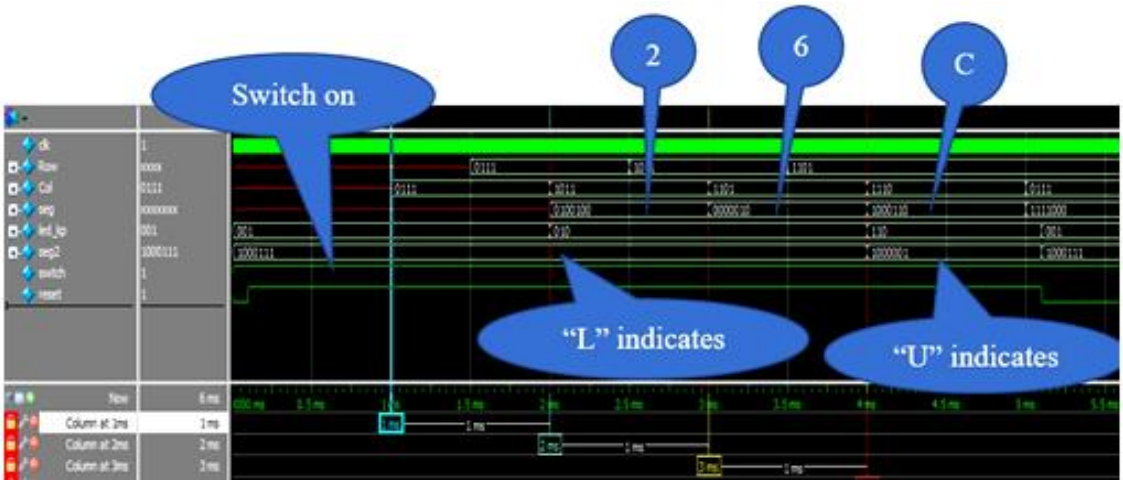


Figure 10. ModelSim simulation when keypad "2", "6" and "c" correctly entered. "L" indicates "Lock" and "U" indicates "Unlock"

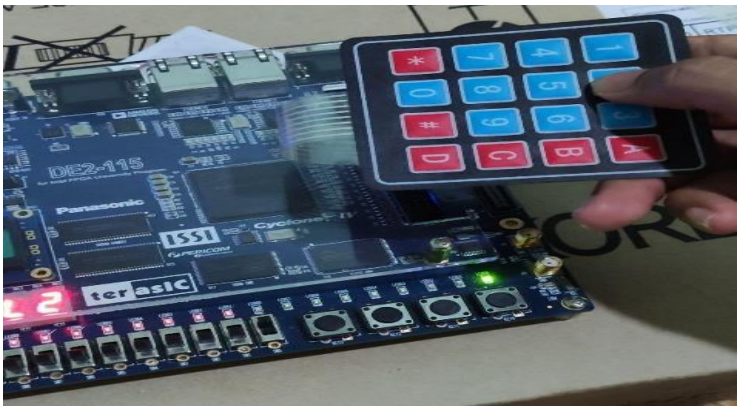


Figure 11. Verification when keypad "2"correctly entered

Figure 12. Verification when keypad "6" correctly entered

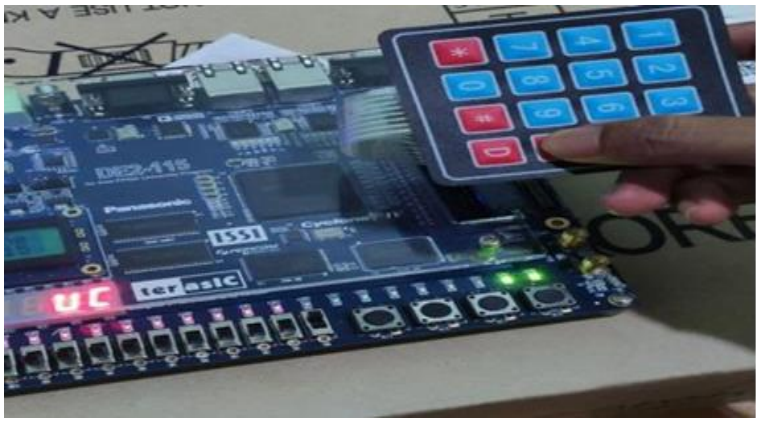


Figure 13. Verification when keypad "C" correctly entered

Table 2. Summary on ModelSim simulation

Switch	Lock Mode				Output	
	Push Button	Keypad			Desired ModelSim	Actual ModelSim
		2	6	C		
0	0	X	X	X	1	1
0	1	X	X	X	0	0
1	0	X	X	X	0	0
1	1	/	/	/	U	U

Table 3. Summary on verification using Altera DE2-115

Switch	Lock Mode				Output	
	Push Button	Keypad			Desired DE2-115	Actual DE2-115
		2	6	C		
0	0	X	X	X	Green LED ON	Green LED ON
0	1	X	X	X	Green LED OFF	Green LED OFF
1	0	X	X	X	Depend on last state	Last state Green LED off
1	1	/	/	/	U	U

4. CONCLUSION

In conclusion, the FSM method has been chosen for this project to design digital hardware circuit of home security code lock using verilog HDL in Quartus II. The design is then simulated to verify the functionality on the digital hardware circuit of home security code lock in ModelSim. By ModelSim, the timing diagram were being observed and analysed to ensure the layout of the design is as desired. Then, download the design onto the Altera DE2-115 trainer board. The observation on the results achieved via the ModelSim simulation and verification via Altera DE2-115 trainer board satisfied the theoretical part in FSM.

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